Claims

What is claimed is:

1. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration in a channel adapter comprising the steps of:

providing a first register for communicating an adapter buffer size and allocation capability for the channel adapter;

providing at least one second register for communicating a current port buffer size; one said second register associated with each physical port of the channel adapter;

providing a plurality of third registers for communicating a current VL buffer size; one said third register associated with each VL of each said physical port of the channel adapter; and

utilizing said second register for receiving change requests for adjusting said current port buffer size for an associated physical port; and

utilizing said third register for receiving change requests for adjusting said current VL buffer size for an associated VL.

2. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein said first register includes predefined fields for storing said adapter buffer size, a flexibly allocated buffer space for the channel adapter, and an allocation unit for buffer allocation.

3. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein each said second register includes predefined fields for storing said current port buffer size, a fixed port buffer space and a requested port buffer size.

4. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein each said third register includes predefined fields for storing said current VL buffer size, a fixed VL buffer space and a requested VL buffer size.

5. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein utilizing said second register for receiving change requests for adjusting said current port buffer size for said associated physical port includes the steps of utilizing a hypervisor for writing said change request to a requested port buffer field of said second register for adjusting said current port buffer size for said associated physical port.

6. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein utilizing third register for receiving change requests for adjusting said current VL buffer size for said associated VL includes the steps of utilizing a hypervisor for writing said change request to a requested VL buffer field of said third register for adjusting said current port buffer size for said associated physical port.

7. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 further includes providing a plurality of change and status registers for communicating VL change and status values; one said change and status register associated with each said VL of each said physical port of the channel adapter register.

8. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 includes providing a hypervisor for monitoring buffer resources, and using said hypervisor for writing change requests to respective ones of each said second register and said third registers.

9. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 further includes providing channel adapter hardware for managing allocation of buffer space responsive to said change requests written by said hypervisor.

10. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein providing said hypervisor for monitoring buffer resources includes providing at least one register for storing VL buffer usage statistics; and said hypervisor periodically polling said at least one register for storing VL buffer usage statistics.

11. Apparatus for implementing dynamic Virtual Lane (VL) buffer reconfiguration comprising:

a first register for communicating an adapter buffer size and allocation capability for a channel adapter;

at least one second register for communicating a current port buffer size; one said second register associated with each physical port of the channel adapter;

a plurality of third registers for communicating a current VL buffer size; one said third register associated with each VL of each said physical port of the channel adapter;

a hypervisor for writing change requests to said second register for adjusting said current port buffer size for an associated physical port; and

said hypervisor for writing change requests to said third register for adjusting said current VL buffer size for an associated VL; and

channel adapter hardware for managing allocation of buffer space responsive to said change requests written by said hypervisor.

12. Apparatus for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 11 wherein said first register includes predefined fields for storing said adapter buffer size, a flexibly allocated buffer space for the channel adapter, and an allocation unit used for buffer allocation.

13. Apparatus for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 11 wherein each said second register includes predefined fields for storing said current port buffer size, a fixed port buffer space and a requested port buffer size; said hypervisor writes said change requests to said requested port buffer size field.

14. Apparatus for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 11 wherein said channel adapter hardware includes buffer management state machine hardware.

15. Apparatus for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 11 wherein each said third register includes predefined fields for storing said current VL buffer size, a fixed VL buffer space and a requested VL buffer size; said hypervisor writes said change requests to said requested VL buffer size field.

16. Apparatus for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 11 includes at least one register storing VL buffer usage statistics; and said hypervisor for monitoring buffer resources and periodically polling said at least one register storing VL buffer usage statistics.

17. A computer program product for implementing dynamic Virtual Lane (VL) buffer reconfiguration in a channel adapter of a system area network, said computer program product including a plurality of computer executable instructions stored on a computer readable medium, wherein said instructions, when executed by the channel adapter, cause the channel adapter to perform the steps of:

communicating an adapter buffer size and allocation capability for the channel adapter using a first register;

communicating a current port buffer size using a second register; one said second register associated with each physical port of the channel adapter;

communicating a current VL buffer size using a third register; one said third register associated with each VL of each said physical port of the channel adapter; and

writing a change request to one said second register for adjusting said current port buffer size for said associated physical port; and

writing a change request to one said third register for adjusting said current VL buffer size for said associated VL.

18. A computer program product as recited in claim 17 wherein said instructions, when executed by the channel adapter, cause the channel adapter to perform the steps of: monitoring buffer resources by periodically polling a register storing VL buffer usage statistics.

19. A computer program product as recited in claim 17 wherein said instructions, when executed by the channel adapter, cause the channel adapter to perform the steps of: writing said change requests responsive to monitoring buffer resources.